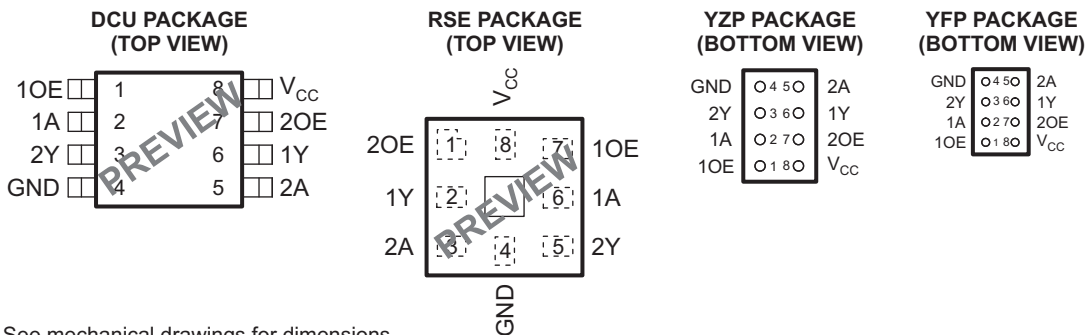


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Low Static-Power Consumption ($I_{CC} = 0.9 \mu\text{A Max}$)
- Low Dynamic-Power Consumption ($C_{pd} = 4 \text{ pF Typ at } 3.3 \text{ V}$)
- Low Input Capacitance ($C_i = 1.5 \text{ pF Typ}$)
- Low Noise – Overshoot and Undershoot <math><10\% \text{ of } V_{CC}</math>
- Input-Disable Feature Allows Floating Input Conditions
- I_{off} Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4.6 \text{ ns Max at } 3.3 \text{ V}$
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figure 1 and Figure 2).

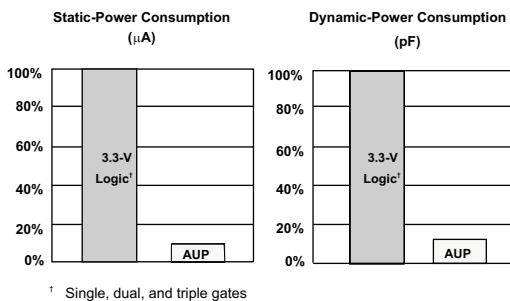


Figure 1. AUP – The Lowest Power Family

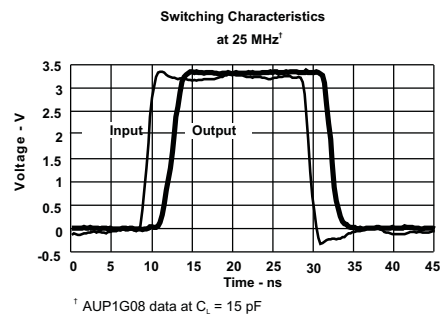


Figure 2. Excellent Signal Integrity



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

SN74AUP2G126

LOW-POWER DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCES687B–JANUARY 2007–REVISED JANUARY 2008

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74AUP2G126 is a dual bus driver/line driver with 3-state outputs, designed for 0.8-V to 3.6-V V_{CC} operation. The outputs are disabled when the associated output-enable (OE) input is low. This device has the input-disable feature, which allows floating input signals.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP2G126YFPR	___ HN_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP2G126YZPR	___ HN_
	QFN – RSE	Reel of 3000	SN74AUP2G126RSER	HN
	VSSOP – DCU	Reel of 3000	SN74AUP2G126DCUR	H26_

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).
DCU: The actual top-side marking has one additional character to designate the assembly/test site.

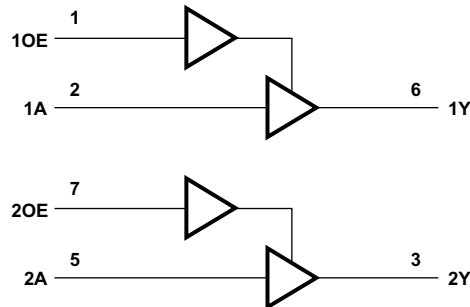
FUNCTION TABLE

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	$X^{(1)}$	Z

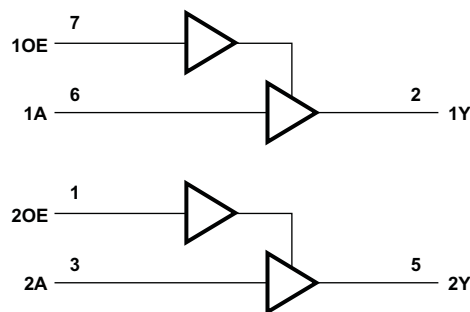
- (1) Floating inputs allowed

LOGIC DIAGRAMS (POSITIVE LOGIC)

DCU, YFP, and YZP Packages



RSE Package



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V
V_O	Output voltage range in the high or low state ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current		-50	mA
I_{OK}	Output clamp current		-50	mA
I_O	Continuous output current		±20	mA
	Continuous current through V_{CC} or GND		±50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DCU package	227	°C/W
		RSE package	253	
		YZP package	102	
		YFP package	98.8	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74AUP2G126

LOW-POWER DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

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RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 0.8\text{ V}$	V_{CC}	3.6
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	3.6
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.6	3.6
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	2	3.6
V_{IL}	Low-level input voltage	$V_{CC} = 0.8\text{ V}$	0	0
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	0	$0.35 \times V_{CC}$
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0	0.7
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	0	0.9
V_O	Output voltage	Active state	0	V_{CC}
		3-state	0	3.6
I_{OH}	High-level output current	$V_{CC} = 0.8\text{ V}$		–20
		$V_{CC} = 1.1\text{ V}$		–1.1
		$V_{CC} = 1.4\text{ V}$		–1.7
		$V_{CC} = 1.65\text{ V}$		–1.9
		$V_{CC} = 2.3\text{ V}$		–3.1
		$V_{CC} = 3\text{ V}$		–4
I_{OL}	Low-level output current	$V_{CC} = 0.8\text{ V}$		20
		$V_{CC} = 1.1\text{ V}$		1.1
		$V_{CC} = 1.4\text{ V}$		1.7
		$V_{CC} = 1.65\text{ V}$		1.9
		$V_{CC} = 2.3\text{ V}$		3.1
		$V_{CC} = 3\text{ V}$		4
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8\text{ V to }3.6\text{ V}$		200
T_A	Operating free-air temperature		–40	85

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -20 μA	0.8 V to 3.6 V	V _{CC} - 0.1			V _{CC} - 0.1		V
	I _{OH} = -1.1 mA	1.1 V	0.75 × V _{CC}			0.7 × V _{CC}		
	I _{OH} = -1.7 mA	1.4 V	1.11			1.03		
	I _{OH} = -1.9 mA	1.65 V	1.32			1.3		
	I _{OH} = -2.3 mA	2.3 V	2.05			1.97		
	I _{OH} = -3.1 mA		1.9			1.85		
	I _{OH} = -2.7 mA	3 V	2.72			2.67		
	I _{OH} = -4 mA		2.6			2.55		
V _{OL}	I _{OL} = 20 μA	0.8 V to 3.6 V				0.1	0.1	V
	I _{OL} = 1.1 mA	1.1 V				0.3 × V _{CC}	0.3 × V _{CC}	
	I _{OL} = 1.7 mA	1.4 V				0.31	0.37	
	I _{OL} = 1.9 mA	1.65 V				0.31	0.35	
	I _{OL} = 2.3 mA	2.3 V				0.31	0.33	
	I _{OL} = 3.1 mA					0.44	0.45	
	I _{OL} = 2.7 mA	3 V				0.31	0.33	
	I _{OL} = 4 mA					0.44	0.45	
I _I	A or OE input	V _I = GND to 3.6 V	0 V to 3.6 V			0.1	0.5	μA
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V			0.2	0.6	μA
ΔI _{off}		V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V			0.2	0.9	μA
I _{OZ}		V _O = V _{CC} or GND	3.6 V			0.1	0.5	μA
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), OE = V _{CC} , I _O = 0	0.8 V to 3.6 V			0.5	0.9	μA
ΔI _{CC}	A input	V _I = V _{CC} - 0.6 V ⁽¹⁾ , I _O = 0	3.3 V			40	50	μA
	OE input					110	120	
	All inputs	V _I = GND to 3.6 V, OE = GND ⁽²⁾	0.8 V to 3.6 V			0	0	
C _I		V _I = V _{CC} or GND	0 V			2		pF
			3.6 V			2		
C _O		V _O = V _{CC} or GND	3.6 V			3		pF

 (1) One input at V_{CC} - 0.6 V, other input at V_{CC} or GND

 (2) To show I_{CC} is very low when the input-disable feature is enabled

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LOW-POWER DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCES687B–JANUARY 2007–REVISED JANUARY 2008

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 5$ pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		19.2				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	0.5	7.5	17.9	0.5	18.7	
			$1.5\text{ V} \pm 0.1\text{ V}$	0.6	5.2	10.8	0.5	12.4	
			$1.8\text{ V} \pm 0.15\text{ V}$	0.8	4.1	8.1	0.5	9.7	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.1	2.9	5	0.5	6.5	
			$3.3\text{ V} \pm 0.3\text{ V}$	0.5	3	9.5	0.5	9.9	
t_{en}	OE	Y	0.8 V		19.6				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	0.5	8.4	20.8	0.5	21.8	
			$1.5\text{ V} \pm 0.1\text{ V}$	0.5	5.6	11.8	0.5	13.7	
			$1.8\text{ V} \pm 0.15\text{ V}$	0.7	4.3	8.8	0.5	10.6	
			$2.5\text{ V} \pm 0.2\text{ V}$	0.9	2.9	5.4	0.5	7	
			$3.3\text{ V} \pm 0.3\text{ V}$	0.5	2.8	8.8	0.5	9.3	
t_{dis}	OE	Y	0.8 V		12.1				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	0.6	5.2	10.9	0.5	11.1	
			$1.5\text{ V} \pm 0.1\text{ V}$	1.1	3.8	7	0.9	7.1	
			$1.8\text{ V} \pm 0.15\text{ V}$	1.9	3.5	5.6	1.6	5.8	
			$2.5\text{ V} \pm 0.2\text{ V}$	0.9	2.5	3.9	0.8	4.2	
			$3.3\text{ V} \pm 0.3\text{ V}$	0.5	3.5	9.3	0.5	9.3	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 10$ pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		23				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	0.5	8.7	20.6	0.5	21.3	
			$1.5\text{ V} \pm 0.1\text{ V}$	1.2	6	12.2	0.5	13.7	
			$1.8\text{ V} \pm 0.15\text{ V}$	1.4	4.8	9.2	0.5	10.8	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.5	3.4	5.8	0.5	7.2	
			$3.3\text{ V} \pm 0.3\text{ V}$	0.5	3.4	8.9	0.5	9.4	
t_{en}	OE	Y	0.8 V		21.9				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	0.5	9.7	23.1	0.5	24	
			$1.5\text{ V} \pm 0.1\text{ V}$	1	6.4	13.2	0.5	15	
			$1.8\text{ V} \pm 0.15\text{ V}$	1	5	9.9	0.5	11.7	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.2	3.4	10.4	0.5	12	
			$3.3\text{ V} \pm 0.3\text{ V}$	0.5	3.2	8.1	0.5	8.7	
t_{dis}	OE	Y	0.8 V		13.4				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	0.8	6.2	12.6	0.6	12.7	
			$1.5\text{ V} \pm 0.1\text{ V}$	2.1	4.6	7.9	1.9	8.1	
			$1.8\text{ V} \pm 0.15\text{ V}$	1.7	4.7	8.2	1.5	8.3	
			$2.5\text{ V} \pm 0.2\text{ V}$	1	3.3	5.1	0.9	5.3	
			$3.3\text{ V} \pm 0.3\text{ V}$	1.2	4.5	7.8	1.1	7.9	

SWITCHING CHARACTERISTICS

 over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V	26.2					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	0.5	9.7	22.7	0.5	23.4	
			$1.5\text{ V} \pm 0.1\text{ V}$	1.7	4.6	13.6	0.5	15	
			$1.8\text{ V} \pm 0.15\text{ V}$	1.7	5.4	10.2	0.5	11.7	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.7	3.9	6.5	0.5	7.9	
			$3.3\text{ V} \pm 0.3\text{ V}$	0.5	3.7	8.4	0.5	8.9	
t_{en}	OE	Y	0.8 V	23					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	0.5	10.5	24.8	0.5	25.6	
			$1.5\text{ V} \pm 0.1\text{ V}$	1.5	7.1	14.3	0.5	16	
			$1.8\text{ V} \pm 0.15\text{ V}$	1.4	5.6	10.8	0.5	12.4	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.6	3.9	6.8	0.5	8.3	
			$3.3\text{ V} \pm 0.3\text{ V}$	0.5	3.6	7.6	0.5	8.3	
t_{dis}	OE	Y	0.8 V	13.6					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	1.1	6.5	12.7	1	12.8	
			$1.5\text{ V} \pm 0.1\text{ V}$	0.5	4.8	9.1	0.5	9.2	
			$1.8\text{ V} \pm 0.15\text{ V}$	1.8	5.4	9.2	1.7	9.3	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.6	3.7	5.5	1.5	5.7	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.8	5.3	7.9	2.7	7.9	

SWITCHING CHARACTERISTICS

 over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V	36.4					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	0.5	13	30.8	0.5	31.2	
			$1.5\text{ V} \pm 0.1\text{ V}$	2.7	9.1	18	1.1	19.1	
			$1.8\text{ V} \pm 0.15\text{ V}$	2.6	7.2	13.6	1	14.8	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.6	5.3	8.6	1.3	9.9	
			$3.3\text{ V} \pm 0.3\text{ V}$	1.4	4.8	7.9	0.7	8.6	
t_{en}	OE	Y	0.8 V	32.8					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	0.5	14.4	32.4	0.5	33.1	
			$1.5\text{ V} \pm 0.1\text{ V}$	2.5	9.7	18.5	1.1	19.9	
			$1.8\text{ V} \pm 0.15\text{ V}$	2.3	7.6	14.3	0.8	15.7	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.4	5.3	9	1.2	10.3	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.8	4.6	7.2	1.7	8.2	
t_{dis}	OE	Y	0.8 V	20.1					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	0.5	10.3	19.3	0.5	19.3	
			$1.5\text{ V} \pm 0.1\text{ V}$	1.9	7.6	14.5	1.8	14.5	
			$1.8\text{ V} \pm 0.15\text{ V}$	3	8.8	14.9	2.8	14.9	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.9	6.5	10	2.9	10.1	
			$3.3\text{ V} \pm 0.3\text{ V}$	0.5	8.2	17.9	0.5	17.9	

SN74AUP2G126 LOW-POWER DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

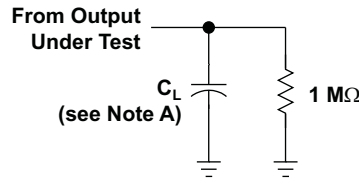
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OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

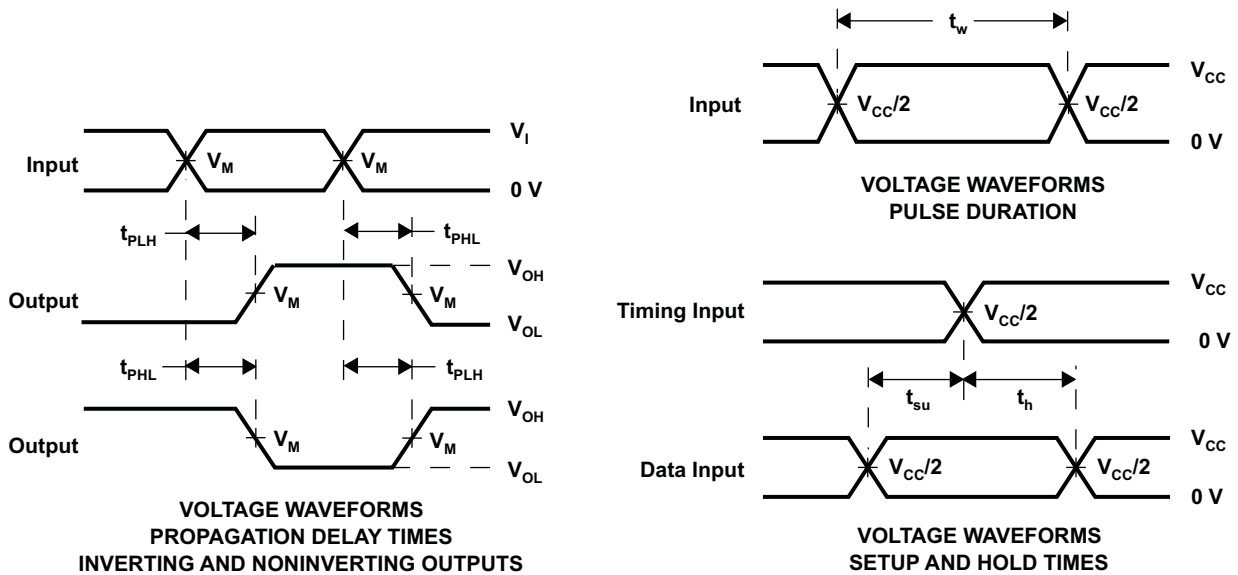
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT	
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	0.8 V	3.8	pF
				$1.2\text{ V} \pm 0.1\text{ V}$	3.7	
				$1.5\text{ V} \pm 0.1\text{ V}$	3.7	
				$1.8\text{ V} \pm 0.15\text{ V}$	3.7	
				$2.5\text{ V} \pm 0.2\text{ V}$	3.9	
				$3.3\text{ V} \pm 0.3\text{ V}$	4	
	Outputs disabled	f = 10 MHz	0.8 V	0		
			$1.2\text{ V} \pm 0.1\text{ V}$	0		
			$1.5\text{ V} \pm 0.1\text{ V}$	0		
			$1.8\text{ V} \pm 0.15\text{ V}$	0		
			$2.5\text{ V} \pm 0.2\text{ V}$	0		
			$3.3\text{ V} \pm 0.3\text{ V}$	0		

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)



LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_i	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



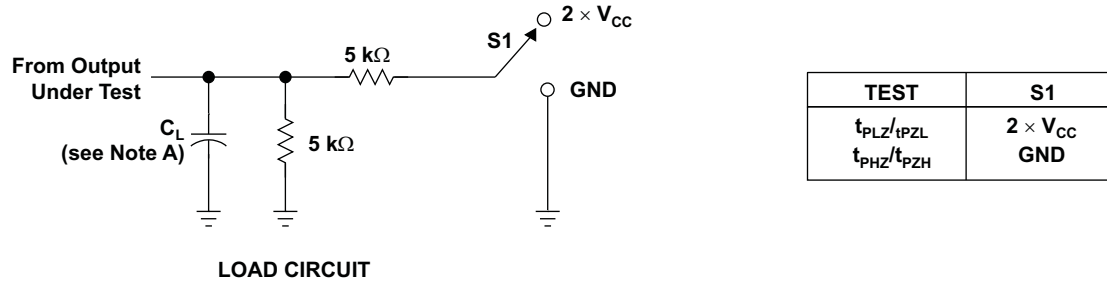
- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
 C. The outputs are measured one at a time, with one transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .
 E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

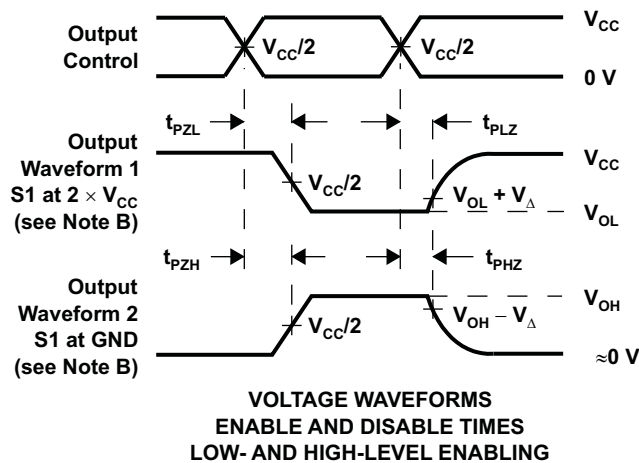
SN74AUP2G126 LOW-POWER DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCES687B—JANUARY 2007—REVISED JANUARY 2008

PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AUP2G126YFPR	ACTIVE	DSBGA	YFP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74AUP2G126YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

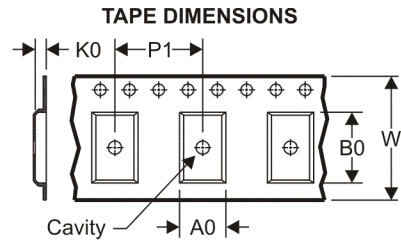
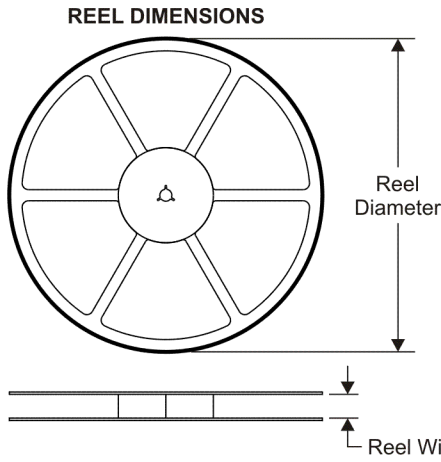
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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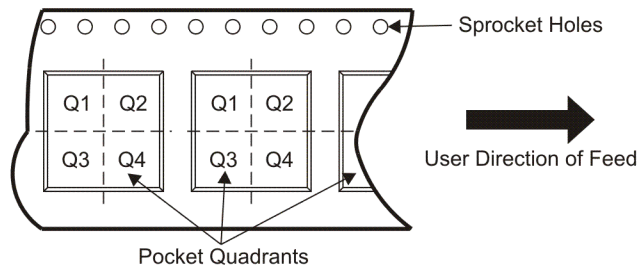
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TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

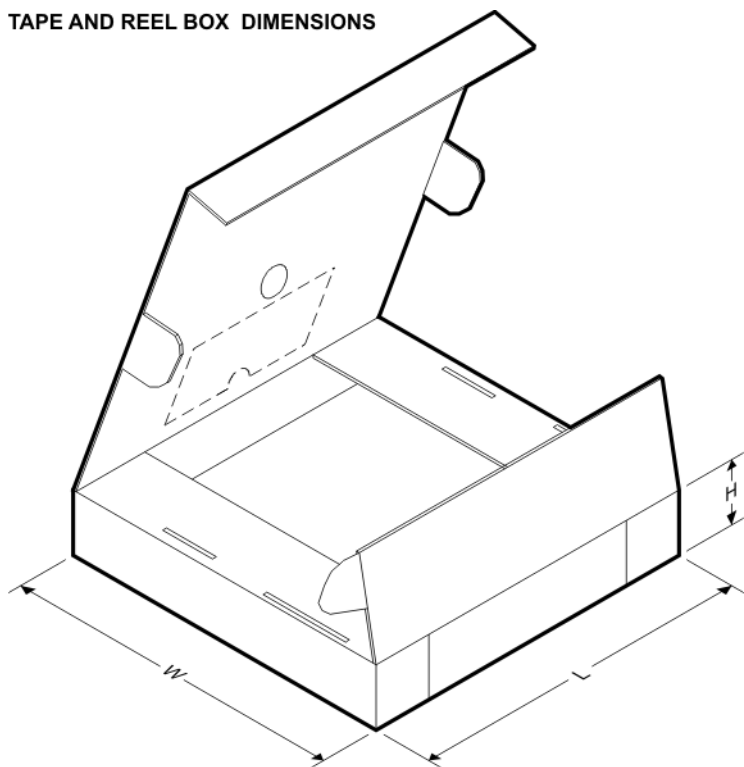
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G126YFPR	DSBGA	YFP	8	3000	180.0	8.4	0.83	1.63	0.59	4.0	8.0	Q1
SN74AUP2G126YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.1	2.1	0.56	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



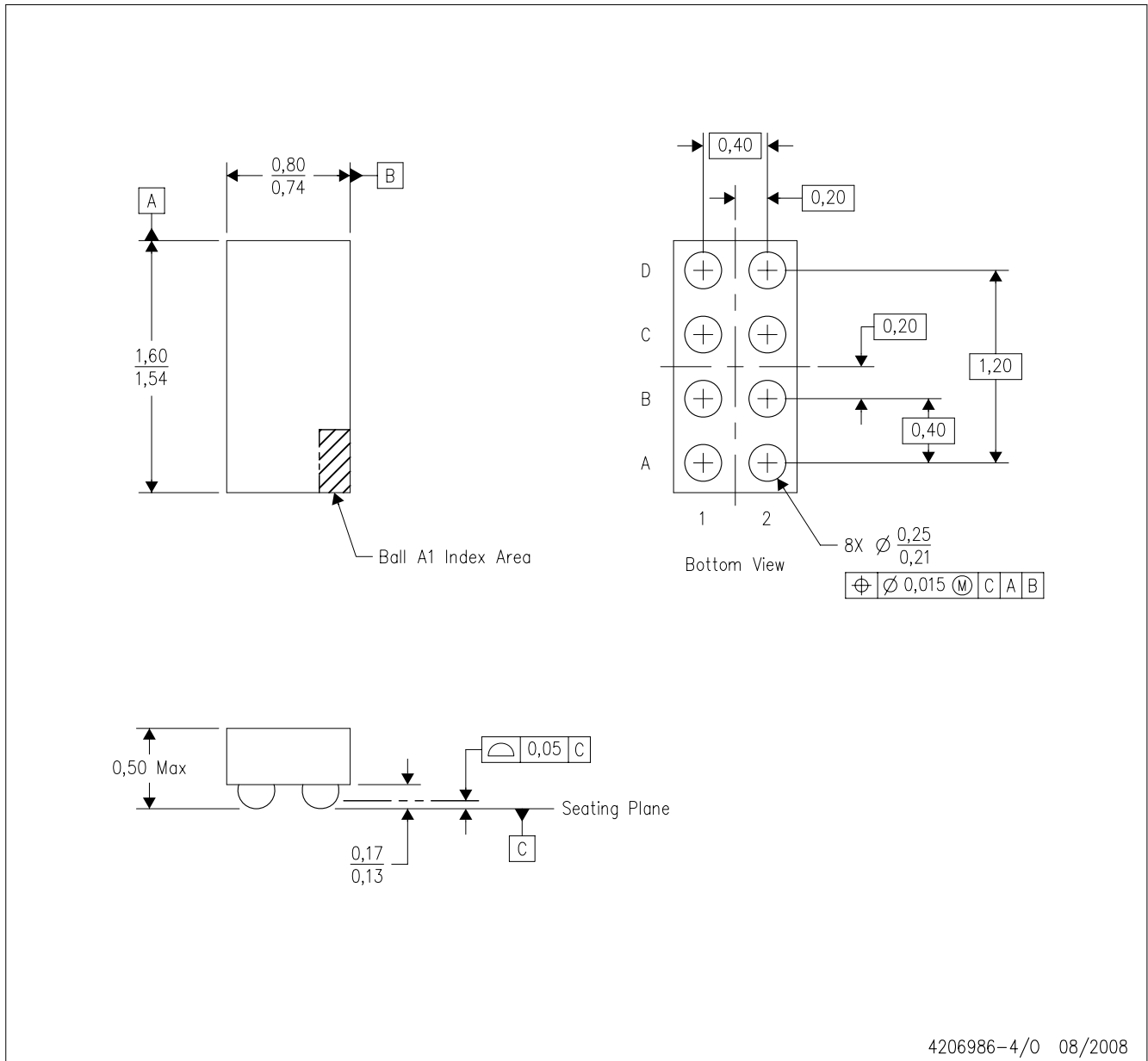
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G126YFPR	DSBGA	YFP	8	3000	220.0	220.0	34.0
SN74AUP2G126YZPR	DSBGA	YZP	8	3000	220.0	220.0	34.0

MECHANICAL DATA

YFP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



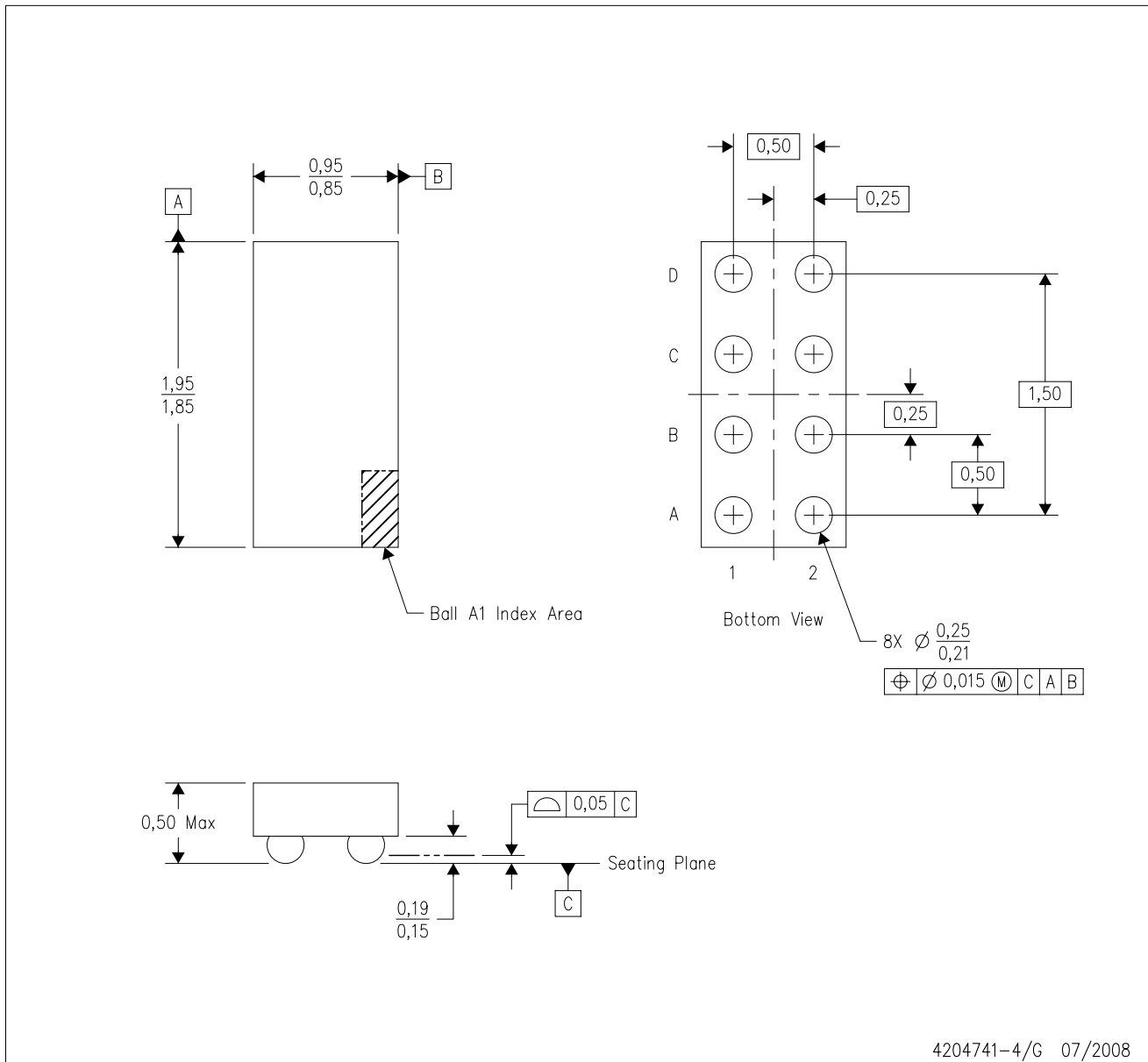
4206986-4/0 08/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This is a Pb-free solder ball design.

NanoFree is a trademark of Texas Instruments.

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

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